2912 FAMILY
PCM LINE FILTERS

		Frequency Response CCITT G712	D3/D4
Idle Channel Noise (dBrncO)	12	2912-3	2912
	14	2912-5	2912-6

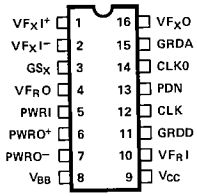
- **AT&T® D3/D4 Compatible and CCITT G712 Compatible**
- **Monolithic Device Includes Both Transmit and Receive Filters**
- **50Hz/60Hz Rejection Included in the Transmit Filter**
- **Gain Adjustment in Both Directions**
- **Direct Interface with Transformer or Electronic Telephone Hybrids**
- **Direct Interface to the Intel® 2910A/2911A PCM Codecs Including Stand-By, Power Down Mode**
- **±5% Power Supplies: +5V, -5V**
- **Low Power Consumption:**
  210mW Typical without Power Amplifiers
  280mW Typical with Power Amplifiers
  55 mW Typical Stand-By
- **Fabricated with Reliable N-Channel MOS Process**

The Intel® 2912 is a fully integrated monolithic device containing the two filters of a PCM line or trunk termination. The device is designed to meet the following objectives:

- To meet AT&T D3/D4 frequency response with the 2912 and 2912-6.
  To meet CCITT frequency response with the 2912-3 and 2912-5.
- To meet the digital Class 5 central office switching systems stringent specifications.
- To be directly compatible with the 2910A and 2911A codecs.
- To simplify interfaces to transformers and hybrids. The primary application for the 2912 is in telephone systems for transmission, switching, or remote concentration.

A switched capacitor filter technique is used to implement the transmit and receive passband filter sections of the 2912. The device is fabricated using Intel's reliable two layer polysilicon NMOS technology. The combination of the switched capacitor technique and the NMOS technology result in a monolithic 2912 filter which is packaged in a standard 16 pin DIP.

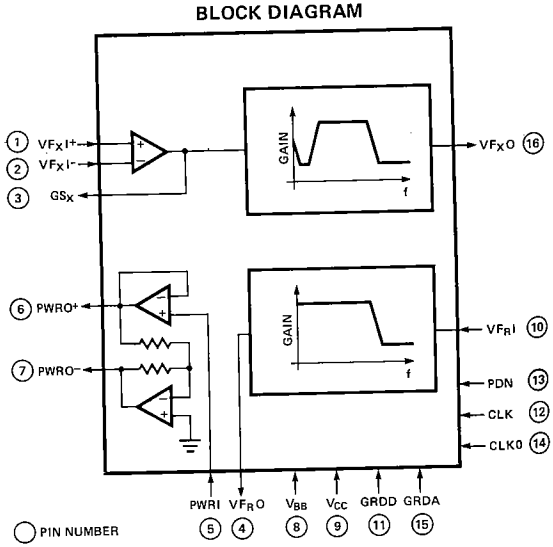
PIN CONFIGURATION



PIN NAMES

VF_XI^+, VF_XI^-	ANALOG INPUTS	CLK	CLOCK INPUT
GS_X	GAIN CONTROL	CLK0	CLOCK SELECTION
VF_XO	ANALOG OUTPUT	PDN	POWER DOWN
VF_RI	ANALOG INPUT	V_{CC}	POWER (+5V)
VF_RO	ANALOG OUTPUT	V_{BB}	POWER (-5V)
PWRI	DRIVER INPUT	GRDD	DIGITAL GROUND
$PWRO^+$, $PWRO^-$	DRIVER OUTPUT	GRDA	ANALOG GROUND

BLOCK DIAGRAM



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PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1	VF_XI^+	Input	Analog input of the transmit filter. The VF_XI^+ signal comes from the 2 to 4 wire hybrid in the case of a 2 wire line and goes through the 50/60Hz notch and the antialiasing filter before being sent to the Codec for encoding.
2	VF_XI^-	Input	Inverting input of the gain adjustment operational amplifier on the transmit filter.
3	GS_X	Output	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
4	VF_RO	Output	Analog output of the receive filter. This output provides a direct interface to electronic hybrids. For a transformer hybrid application, VF_RO is tied to PRWI and a dual balanced output is provided on pins $PWRO^+$ and $PWRO^-$.
5	PWRI	Input	Input to the power driver amplifiers on the receive side for interface to transformer hybrids. High impedance input. When tied to V_{BB}, the power amplifiers are powered down.
6	$PWRO^+$	Output	Non-inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
7	$PWRO^-$	Output	Inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
8	V_{BB}	Power	-5V ± 5% referenced to GRDA
9	V_{CC}	Power	+5V ± 5% referenced to GRDA
10	VF_RI	Input	Analog input of the receive filter, interface to the Codec analog output for PCM applications. The receive filter provides the $\frac{Sinx}{x}$ correction needed for sample and hold type Codec outputs to give unity gain. The input voltage range is directly compatible with the Intel® 2910A and 2911A Codecs.
11	GRDD	Ground	Digital ground return for internal clock generator.
12	CLK[1]	Input	Clock input. Three clock frequencies can be used: 1.536MHz, 1.544MHz or 2.048MHz; pin 14, CLK0, has to be strapped accordingly. High impedance input, TTL voltage levels.
13	PDN	Input	Control input for the stand-by power down mode. An internal pull up to +5V is provided for interface to the Intel® 2910A and 2911A PDN outputs. TTL voltage levels.
14	CLK0[1]	Input	Clock (pin 12, CLK) frequency selection. If tied to V_{BB}, CLK should be 1.536MHz. If tied to Ground, CLK should be 1.544 MHz. If tied to V_{CC}, CLK should be 2.048MHz.
15	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
16	VF_XO	Output	Analog output of the transmit filter. The output voltage range is directly compatible with the Intel® 2910A and 2911A Codecs.

NOTE:

1. The three clock frequencies are directly compatible with the Intel® 2910A and 2911A Codecs. The following table should be observed in selecting the clock frequency.

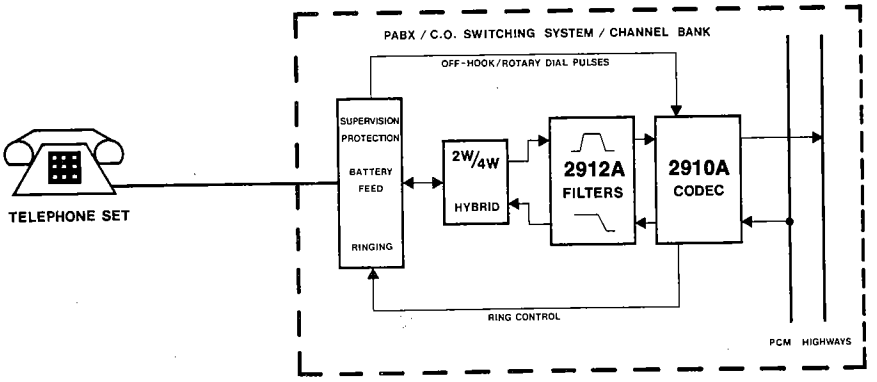
Codec Clock	Clock Bits/Frame	2912 CLK, Pin 12	2912 CLK0, Pin 14
1.536 MHz	192	1.536 MHz	V_{BB} (-5V)
1.544 MHz	193	1.544 MHz	GRDD
2.048 MHz	256	2.048 MHz	V_{CC} (+5V)

FUNCTIONAL DESCRIPTION

The 2912 provides the transmit and receive filters found on the analog termination of a PCM line or trunk. The transmit filter performs the anti-aliasing function needed for an 8kHz sampling system, and the 50/60Hz rejection. The receive filter has a low pass transfer characteristic and also provides the Sinx/x correction necessary to interface the Intel 2910A (μ Law) and 2911A (A Law) Codecs which have a non-return-to-zero output of the digital to analog conversion. Gain adjustment is provided in the receive and transmit directions.

A stand-by, power down mode is included in the 2912 and can be directly controlled by the 2910A/2911A Codecs.

The 2912 can interface directly with a transformer hybrid (2 to 4 wire conversion) or with electronic hybrids; in the latter case the power dissipation is significantly reduced by powering down the output amplifier provided on the 2912.

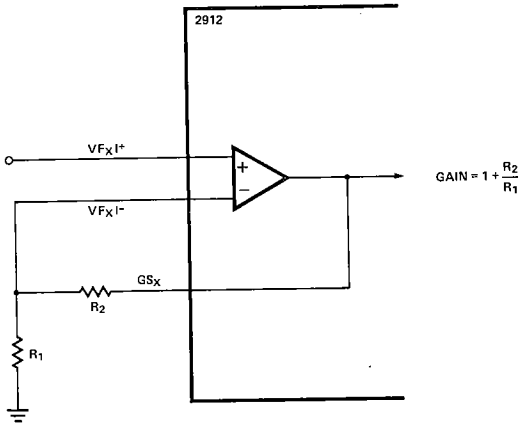


TYPICAL LINE TERMINATION

FILTER OPERATION

Transmit Filter Input Stage

The input stage provides gain adjustment in the passband. The input operational amplifier has a common mode range of ±2.2 volts, a DC offset of less than 25mV, a voltage gain greater than 1000 and a unity gain bandwidth of 1 MHz. It can be connected to provide a gain of 20dB without degrading the noise performance of the filter. The load impedance connected to the amplifier output must be greater than 10KΩ in parallel with 20pF. The input signal on lead $VFxI^+$ can be either AC or DC coupled. The input Op Amp can also be used in the inverting mode or differential amplifier mode. The remaining portion of the transmit filter provides a gain of +3dB in the pass band.



TRANSMIT FILTER GAIN ADJUSTMENT

50Hz/60Hz Notch — Transmit Filter

The transmit filter has a notch section to reject 50Hz and 60Hz components of the input signal. A minimum attenuation of 22dB is provided at 60Hz. At 50Hz, the minimum attenuation is 20dB. The gain at 200Hz is between -.125dB and -1.8dB. (All gain figures are relative to the gain at 1kHz).

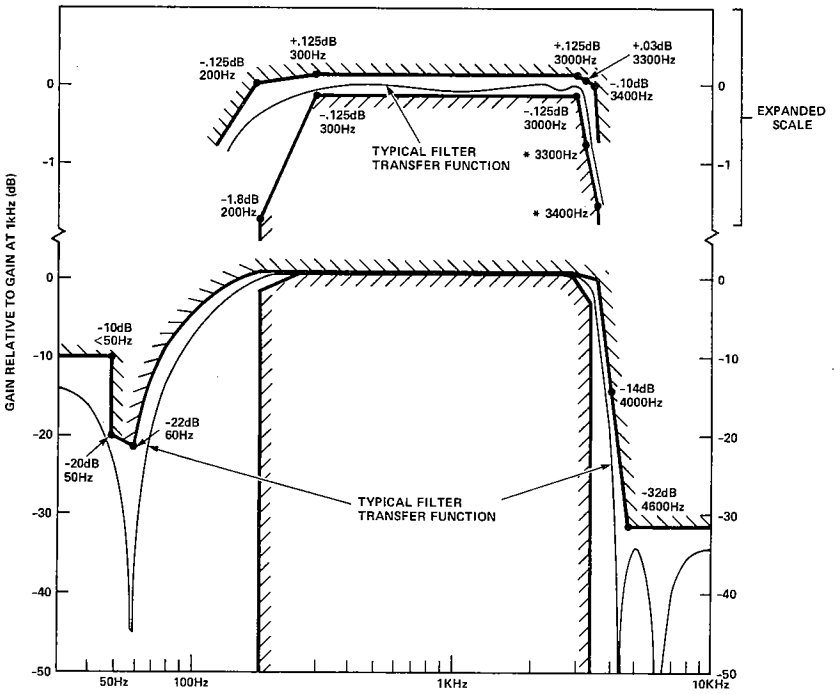
An active RC low pass anti-aliasing filter is included on chip immediately in front of the 50 Hz/60 Hz notch section. This filter provides greater than 35dB attenuation at 256 KHz. As a result no external anti-aliasing components are required to provide the necessary anti-aliasing function for the switched capacitor sections of the transmit filter which operate at an internal sampling rate of 256 KHz.

Transmit Filter Transfer Characteristics

The transmit section of the filter provides a passband flatness and stopband attenuation which exceeds the ATT® D3 and D4 specification (2912 and 2912-6) and the CCITT G712 recommendation (2912-3 and 2912-5). The 2912 specification meets the digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications are shown in the diagram below.

Transmit Filter Output Stage

The voltage range of the output signal on the VF_XO lead is ±3.2 volts. The DC offset is less than 250mV. It is recommended that the VF_XO output be capacitively coupled to the VF_X input of the Intel® 2910A and 2911A Codecs.



* FREQ	2912 2912-6 D3/D4	2912-3 2912-5 CCITT
3300Hz	-.65dB	-.35dB
3400Hz	-1.4	-.70

TRANSMIT FILTER TRANSFER CHARACTERISTICS

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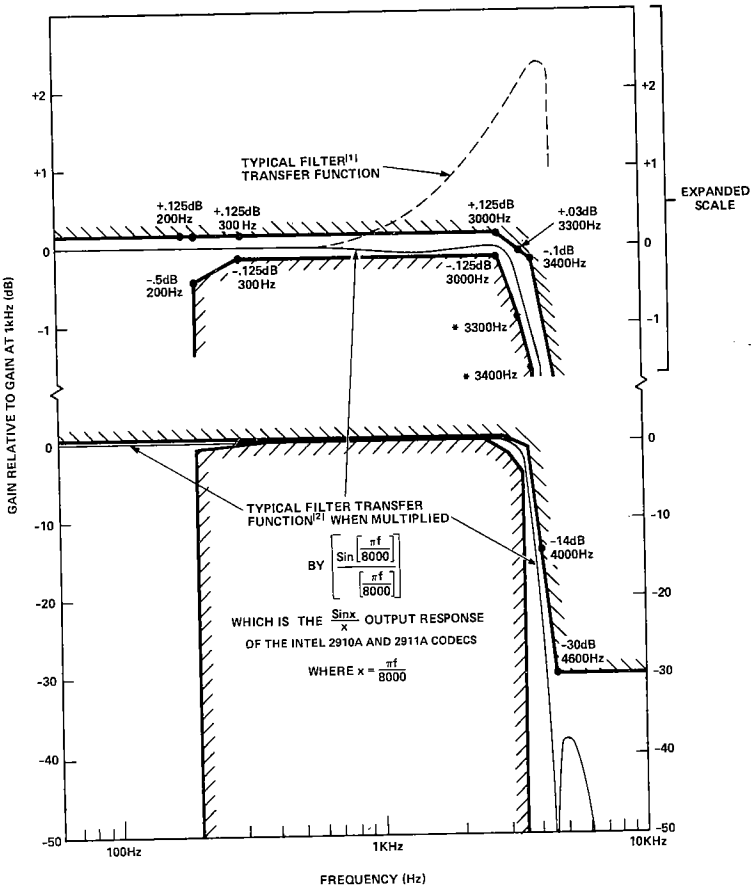
An active RC low pass smoothing filter is included on chip following the transmit filter section. This filter provides reduction of broad band noise and clock noise from the switched capacitor transmit filter section.

As a result (in pleziosynchronous operation where the transmit and receive clocks of the codec are allowed to have a small relative frequency difference, as in transmission applications) low frequency asynchronism between the clock signal in the transmit filter output and the sampling process in the associated codec has negligible effect on the idle channel noise of the codec. This smoothing filter also serves to reduce high frequency broadband noise at the filter output which might be aliased to lower frequencies by the codec sampling process.

Receive Filter Transfer Characteristics

The receive section of the filter provides a passband flatness and stopband rejection which exceeds at ATT® D3/D4 specification (2912 and 2912-5) and the CCITT G712 recommendation (2912-3 and 2912-6) when used with a decoder which contains a sample/hold amplifier at its output. The filter contains the required compensation for the $\frac{Sinx}{x}$ response of such decoders. The receive filter transfer characteristics and specifications, including the $\frac{Sinx}{x}$ response of the decoder, are shown in the diagram below.



NOTES:
1. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER AS A SEPARATE COMPONENT.
2. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER DRIVEN BY THE SAMPLE AND HOLD OUTPUT OF THE INTEL 2910A AND 2911A CODECS. THE COMBINED FILTER/CODEC RESPONSE MEETS THE STATED SPECIFICATIONS.

* FREQ	2912 2912-6 D3/D4	2912-3 2912-5 CCITT
3300Hz	-.65dB	-.35dB
3400Hz	-1.4	-.70

RECEIVE FILTER TRANSFER CHARACTERISTICS

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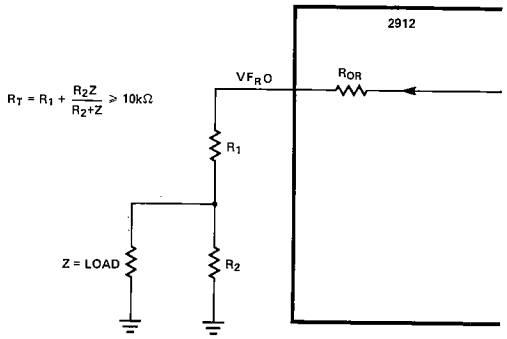
Receive Filter Output

The VF_RO lead is capable of driving high impedance electronic hybrids. The gain of the receive section from VF_RI to VF_RO is:

$$\frac{\left(\frac{\pi f}{8000}\right)}{\sin\left(\frac{\pi f}{8000}\right)}$$

which when multiplied by the output response of the Intel 2910A and 2911A Codecs results in a 0dB gain in the passband. The filter gain can be adjusted downward by a resistor voltage divider connected as shown. The total resistive load R_T on VF_RO should not be less than 10kΩ.

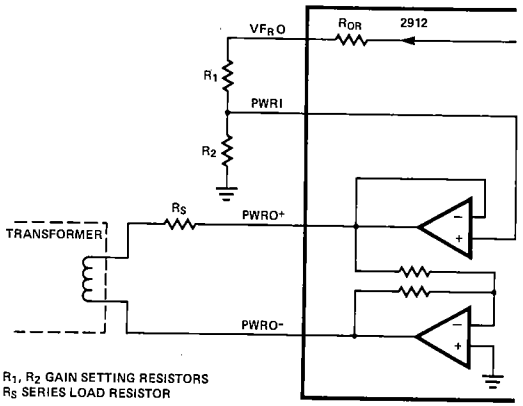


RECEIVE FILTER OUTPUT GAIN ADJUSTMENT

Receive Filter Output Driver Amplifier Stage

A balanced power amplifier is provided in order to drive low-impedance loads in a bridged configuration. The receive filter output VF_RO is connected through gain setting resistors R_1 and R_2 to the amplifier input PWRI. The input voltage range on PWRI is ±3.2 volts and the gain is 6dB for a bridged output. With a 20kΩ load connected between $PWRO^+$ and $PWRO^-$, the maximum voltage swing across the load is ±6.4 volts. With a 600Ω load connected between $PWRO^+$ and $PWRO^-$, the maximum voltage swing across the load is ±5.0 volts. The series combination of R_S and the hybrid transformer must present a minimum A.C. load resistance of 600Ω to the amplifier in the bridged configuration. A typical connection of the output driver amplifiers is shown below. These amplifiers can also be used with loads connected to ground.

When the power amplifier is not needed it should be deactivated to save power. This is accomplished by tying the PWRI pin to V_{BB} before the device is powered up.



TYPICAL CONNECTION OF OUTPUT DRIVER AMPLIFIER

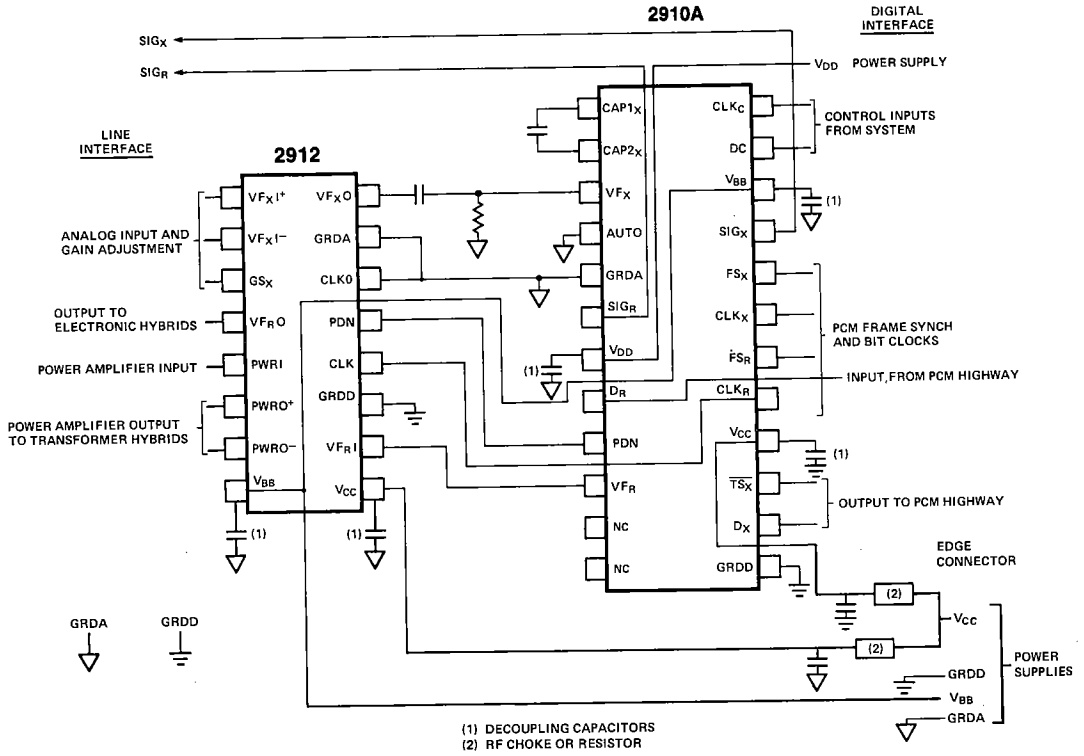
Power Down Mode

Pin 13, PDN, provides the power down control. When the signal on this lead is brought high, the 2912 goes into a standby, power down mode. Power dissipation is reduced to 55mW. In the stand-by mode, all outputs go into a high impedance state. This feature allows multiple 2912's to drive the same analog bus on a time-shared basis.

When power is restored, the settling time of the 2912 is typically 15ms.

The PDN interface is directly compatible with the Intel 2910A and 2911A PDN outputs. Only one command from the common control is then necessary to power down both the Codec and the Filters of the line or trunk interface.

APPLICATIONS
Circuit Interface



A TYPICAL 2910A CODEC AND 2912 FILTER CONFIGURATION

Codec Interface

The 2912 PCM Filter is designed to directly interface to the 2910A and 2911A Codecs as shown above. The transmit path is completed by connecting the VF_XO output of the 2912 to the coupling capacitor associated with the VF_X input of the 2910A and 2911A codecs. The receive path is completed by directly connecting the codec output VF_R to the receive input of the 2912 VF_RI. The PDN input of the 2912 should be connected to the PDN output of the codec to allow the filter to be put in the power-down standby mode under control of the codec.

Clock Interface

To assure proper operation, the CLK input of the 2912 should be connected to the same clock provided to the receive bit clock, CLK_R of 2910A or 2911A Codec as shown above. The CLK0 input of the 2912 should be set to the proper voltage depending on the standard clock frequency chosen for the codec and filter. See the clock selection table in the Pin Description section.

Layout Guidelines

The most important steps in designing a low noise line card are to insure that the layout of the circuit components and traces result in a minimum of cross coupling between analog and digital signals, and to provide well bypassed and clean power supplies, solid ground planes, and minimal lead lengths between components. Considering these items in more detail:

- All power source leads should be bypassed to ground on each printed circuit board (PCB), on which codecs are provided. At least one electrolytic bypass capacitor (at least 10 microfarad) per board is recommended at the point where each power trace from the codec and filter joins prior to interfacing with the edge connector pins assigned to the power leads.

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Layout Guidelines (Cont.)

- Layout the traces on codec and filter equipped boards such that analog signal and capacitor leads are separated as widely as possible from the digital clock and data leads.
- Connect the codec sample and hold capacitor(s) with the shortest leads possible. Mount them as close to the device pins as can be achieved. Shield the capacitor traces with analog ground.
- Do not layout any board traces (especially digital) that pass between or near the leads of the sample and hold capacitor(s) since they are in high impedance circuits which are sensitive to noise coupling.
- Keep analog traces situated in their layouts so that no intervening circuit leads are permitted to run parallel to or between them.
- The optimum grounding configuration is to maintain separate digital and analog grounds on the circuit boards, and to carry these grounds back to the power supply ground with a low impedance connection. This keeps the grounds separate over the entire system except at that one location.
- The voltage difference between ground leads GRDA and GRDD (analog and digital ground) should not exceed two volts. One method of preventing any substantial voltage difference between leads GRDA and GRDD is to connect two diodes back to back in opposite directions across these two ground leads on each board.
- Codec-filter pairs should be aligned so that pins 9 through 16 of the filter face pins 1 through 12 of the codec. This minimizes the distance for analog connections between devices and prevents crossing analog lines.
- No digital lines or high level analog lines should run under or in parallel with analog interconnections from codec to filter. If the analog lines are on top (component side) of the PCB, then GRDD, GRDA, or power supply leads should be directly under them, on the bottom of the PCB (to prevent analog/digital coupling).
- Both the codec and filter devices should be shielded from traces on the bottom of the PCB by using ground or power supply leads on the top side directly under the device (like a ground plane).
- For each printed circuit board, two +5 volt power supply leads should be used, one for codecs and the other for filters, and separately decoupled where they join a single 5 volt supply at the PCM connector. Decoupling can be accomplished with a RC lowpass filter or a RF choke per power supply input. Both grounds and power leads must have low resistance and inductance which can be accomplished by using a ground plane whenever possible. If narrower traces must be used, maintain a minimum width of 4 millimeters and use multiple or extra large plated holes when passing ground connections through the PCB.
- The 2912 PCM filter should have all power supplies bypassed to analog ground (GRDA). The 2910A/11A codec +5V power supplies should be bypassed to the digital ground (GRDD) but the −5V and +12V supplies should be bypassed to analog ground (GRDA).

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage with Respect to V_{BB} .. -0.3V to +14.0V
All Input and Output Voltages with
Respect to V_{BB} ..... -0.3V to +14.0V
All Output Currents ..... ±50mA
Power Dissipation ..... 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

DIGITAL INTERFACE

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_{LIC}	Input Load Current (except PDN)			10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LIO}	Input Load Current, CLK0			10	μA	V_{IN} = V_{BB} to $V_{IH\ MAX}$
I_{LIP}	Input Load Current, PDN			-100	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
V_{IL}	Input Low Voltage (except CLK0)			0.8	V	
V_{IH}	Input High Voltage (except CLK0)	2.2			V	
V_{IL0}	Input Low Voltage, CLK0	V_{BB}		V_{BB}+0.5	V	
V_{Ii0}	Input Intermediate Voltage, CLK0	GRDD-0.5		0.8	V	
V_{IH0}	Input High Voltage, CLK0	V_{CC}-0.5		V_{CC}	V	

POWER DISSIPATION

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_{CC0}	V_{CC} Standby Current		6	9	mA	PDN = $V_{IH\ MIN}$
I_{BB0}	V_{BB} Standby Current		5	9	mA	PDN = $V_{IH\ MIN}$
I_{CC1}	V_{CC} Operating Current, Power Amplifiers Inactive		21	34	mA	PWRI = V_{BB}
I_{BB1}	V_{BB} Operating Current, Power Amplifiers Inactive		21	34	mA	PWRI = V_{BB}
I_{CC2}	V_{CC} Operating Current		28	44	mA	
I_{BB2}	V_{BB} operating Current		28	44	mA	

NOTE: 1. Typical values are for T_A = 25°C and nominal power supply values.

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D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{BRA}	Input Leakage Current, PWRI			3	μA	-3.2V < V_{IN} < 3.2V
R_{IRA}	Input Resistance, PWRI	10			MΩ	
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	$\|I_{OUT}\|$ <10mA -3.0V < V_{OUT} < 3.0V
V_{OSRA}	Output DC Offset, PWRO+, PWRO−			75	mV	PWRI Connected to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF	
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO− Single Ended Connection			±3.2	V	R_L = 10kΩ
				±2.9	V	R_L = 600Ω
				±2.5	V	R_L = 300Ω
						R_L Connected to GRDA
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO− Balanced Output Connection			±6.4	V	R_L = 20kΩ
				±5.8	V	R_L = 1200Ω
				±5.0	V	R_L = 600Ω
						R_L Connected Between PWRO+ and PWRO−

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Clock Input Frequency: CLK = 1.536MHz ± 0.1%, CLK0 = V_{IL0} (Tied to V_{BB}) CLK = 2.048MHz ± 0.1%, CLK0 = V_{IH0} (Tied to V_{CC})
CLK = 1.544MHz ± 0.1%, CLK0 = V_{IL0} (Tied to GRDD)

TRANSMIT FILTER TRANSFER CHARACTERISTICS

(See Transmit Filter Transfer Characteristics description section for graph)

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
G_{RX}	Gain Relative to Gain at 1kHz					0dBmO Input Signal
	Below 50Hz			-10	dB	Gain Setting Op Amp at
	50Hz			-20	dB	Unity Gain
	60Hz			-22	dB	
	200Hz	-1.8		-0.125	dB	0dBmO Signal ≡ 1.1 V_{RMS}
	300Hz to 3000Hz	-0.125		0.125	dB	Input at VF_XI-
	3300Hz	-0.65		0.03	dB	
	3300Hz (2912-3 & 2912-5)	-.35		0.03	dB	
	3400Hz	-1.4		-0.1	dB	0dBmO Signal ≡ 1.6 V_{RMS}
	3400Hz (2912-3 & 2912-5)	-0.7		-0.1	dB	Output at VF_XO
	4000Hz			-14	dB	
	4600Hz and Above			-32	dB	
G_{AX}	Absolute Passband Gain at 1kHz, VF_XO	2.9	3.0	3.1	dB	R_L = ∞, Note 3
G_{AXT}	Gain Variation with Temperature at 1kHz		.0002		dB/°C	0dBmO Signal Level
G_{AXS}	Gain Variation with Supplies at 1kHz		.04		dB/V	0dBmO Signal Level, Supplies ±5%
CT_{RT}	Cross Talk, Receive to Transmit, Measured at VF_XO $20 \log \frac{VF_XO}{VF_RO}$			-60	dB	VF_RI = 1.6 V_{RMS}, 1kHz Input VF_XI+, VF_XI- Connected to GS_X, GS_X Connected through 10kΩ to GRDA
N_{CX1}	Total C Message Noise at Output, VF_XO 2912, 2912-3		9	12	dBrnc0	Gain Setting Op Amp at
	2912-6, 2912-5		13	14	[2]	Unity Gain
N_{CX2}	Total C Message Noise at Output, VF_XO 2912, 2912-3		10	13	dBrnc0	Gain Setting Op Amp at
	2912-6, 2912-5		14	15	[2]	20dB Gain
D_{DX}	Differential Envelope Delay, VF_XO 1kHz to 2.6kHz			80	μs	
D_{AX}	Absolute Delay at 1kHz, VF_XO			150	μs	
DP_{X1}	Single Frequency Distortion Products			-48	dB	0dBm Input Signal at 1kHz
DP_{X2}	Single Frequency Distortion Products at Maximum Signal Level of +3dBm0 at VF_XO			-45	dB	0.16 V_{RMS} 1kHz Input Signal at VF_XI+; Gain Setting Op Amp at 20dB Gain. The +3dBmO signal at VF_XO is 2.24 V_{RMS}.

See next page for NOTES.

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D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

ANALOG INTERFACE, TRANSMIT FILTER INPUT STAGE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{BXI}	Input Leakage Current, $VFxI^+$, $VFxI^-$			100	nA	-2.2V < V_{IN} < 2.2V
R_{IXI}	Input Resistance, $VFxI^+$, $VFxI^-$	10			MΩ	
V_{OSXI}	Input Offset Voltage, $VFxI^+$, $VFxI^-$			25	mV	-2.2V < V_{IN} < 2.2V
$CMRR_1$	Common Mode Rejection, $VFxI^+$, $VFxI^-$	45			dB	-1.6V < V_{IN} < 1.6V, 0dBmO ≡ 1.1 V_{RMS}, Input at $VFxI^-$
$CMRR_2$	Common Mode Rejection, $VFxI^+$, $VFxI^-$	40			dB	-2.2V < V_{IN} < 2.2V
A_{VOL}	DC Open Loop Voltage Gain, GSx	1000				
fc	Open Loop Unity Gain Bandwidth, GSx		1		MHz	
V_{OXI}	Output Voltage Swing, GSx			±2.5	V	R_L ≥ 10kΩ
C_{LXI}	Load Capacitance, GSx			20	pF	
R_{LXI}	Minimum Load Resistance, GSx	10			kΩ	Minimum R_L

ANALOG INTERFACE, TRANSMIT FILTER

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
R_{OX}	Output Resistance, VFxO			400	Ω	
V_{OSX}	Output DC Offset, VFxO			250	mV	$VFxI^+$ Connected to GRDA, Input Op Amp at Unity Gain
$PSRR_1$	Power Supply Rejection of V_{CC} at 1kHz, VFxO	25	35		dB	Note 2
$PSRR_2$	Power Supply Rejection of V_{BB} at 1kHz, VFxO	25	30		dB	Note 2
C_{LX}	Load Capacitance, VFxO			20	pF	
R_{LX}	Minimum Load Resistance, VFxO	10			kΩ	Minimum R_L
V_{OX}	Output Voltage Swing, 1kHz, VFxO			±3.2	V	R_L≥10KΩ or with 2910A or 2911A

ANALOG INTERFACE, RECEIVE FILTER

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{BR}	Input Leakage Current, VFRI			1	μA	-3.2V < V_{IN} < 3.2V
R_{IR}	Input Resistance, VFRI	1			MΩ	
R_{OR}	Output Resistance, VFRO			100	Ω	
V_{OSR}	Output DC Offset, VFRO			200	mV	VFRI Connected to GRDA
$PSRR_3$	Power Supply Rejection of V_{CC} at 1kHz, VFRO	25	35		dB	
$PSRR_4$	Power Supply Rejection of V_{BB} at 1kHz, VFRO	25	30		dB	
C_{LR}	Load Capacitance, VFRO			20	pF	
R_{LR}	Minimum Load Resistance, VFRO	10			kΩ	Minimum R_L
V_{OR}	Output Voltage Swing, VFRO			±3.2	V	R_L = 10kΩ

NOTE:
1. Typical values for T_A = 25°C and nominal power supply values.
2. $PSRR_{1,2}$ include input op amp in transmit section.

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A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Clock Input Frequency: CLK = 1.536MHz ± 0.1%, CLK0 = V_{IL0} (Tied to V_{BB})
CLK = 1.544MHz ± 0.1%, CLK0 = V_{II0} (Tied to GRDD)
CLK = 2.048MHz ± 0.1%, CLK0 = V_{IH0} (Tied to V_{CC})

RECEIVE FILTER TRANSFER CHARACTERISTICS (See Receive Filter Transfer Characteristics description section for graph)

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
G_{RR}	Gain Relative to Gain at 1kHz with Sinx/x Correction of 2910A or 2911A					0dBmO Input Signal
	Below 200Hz			0.125	dB	0dBmO Signal ≡ 1.6 V_{RMS} x $\left(\text{Sin}\ \frac{f}{2\pi(8000)} \Big/ \frac{f}{2\pi(8000)}\right)$ Input at VF_R I
	200Hz	-0.5		0.125	dB	
	300Hz to 3000Hz	-0.125		0.125	dB	
	3300Hz	-0.65		0.03	dB	
	3300Hz (2912-3 & 2912-5)	-.35		0.03	dB	
	3400Hz	-1.4		-0.1	dB	
	3400Hz (2912-3 & 2912-5)	-0.7		-0.1	dB	
	4000Hz			-14	dB	
	4600Hz and Above			-30	dB	
G_{AR}	Absolute Passband Gain at 1kHz, VF_RO	-0.1	0	+0.1	dB	R_L = ∞, Note 3
G_{ART}	Gain Variation with Temperature at 1kHz		.0002		dB/°C	0dBmO Signal Level
G_{ARS}	Gain Variation with Supplies at 1kHz		.04		dB/V	0dBmO Signal Level, Supplies ±5%
CT_{TR}	Cross Talk, Transmit to Receive, Measured at VF_RO; 20 log (VF_RO/VF_XO)			-60	dB	VF_XI = 1.1 V_{RMS}, 1kHz Output. VF_RI Connected to GRDA.
N_{CR}	Total C Message Noise at Output, VF_RO 2912, 2912-3		9	12	dBrnc0 [2]	VF_RO Output or $PWRO^+$ and $PWRO^-$ Connected with Unity Gain
	2912-6, 2912-5		13	14		
D_{DR}	Differential Envelope Delay, VF_RO, 1kHz to 2.6kHz			100	μs	
D_{AR}	Absolute Delay at 1kHz, VF_RO			110	μs	
DP_{R1}	Single Frequency Distortion Products			-48	dB	0dBm Input Signal at 1kHz
DP_{R2}	Single Frequency Distortion Products at Maximum Signal Level of +3dBmO at VF_RO			-45	dB	+3dBmO Signal Level of 2.24 V_{RMS}, 1kHz Input at VF_RO

NOTES:
1. Typical values are for T_A = 25°C and nominal power supply values.
2. A noise measurement of 18dBrnc into a 600Ω load at the 2912 device is equivalent to 12dBrnc0.
3. For gain under load refer to output resistance specs and perform gain calculation.